OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	06720.0086-01	Serial No.	TO BE ASSIGNED
Applicant	Chyh-Yih CHANG		
Filing Date	September 25, 2003	Group:	TO BE ASSIGNED

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
JS		6,258,634	07/10/2001	Wang et al.			
		5,910,874	06/08/1999	Iniewski et al.			
		5,646,808	07/08/1997	Nakayama			
		5,519,242	05/21/1996	Avery			
		5,631,793	05/20/1997	Ker et al.			
		5,811,857	09/22/1998	Assaderaghi et al.			
		5,502,328	03/26/96	Chen et al.			
		5,581,104	12/03/96	Lowrey et al.			
JS		5,990,520	11/23/99	Noorlag et al.			

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JS	M-D. KER, et al., "CMOS On-Chip ESD Protection Design with Substrate-triggering Technique," Proc. of ICECS, Vol. 1, pp. 273-276, 1998
JS	C. Duvvury et al., "Dynamic Gate Coupling for NMOS for Efficient Output ESD Protection", Proc. of IRPS, pp. 141-150, 1992

Examiner		Date Considered	5-11-5

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JY		5,932,918	08/03/99	Krakauer			
JY		6,015,992	01/18/00	Chatterjee et al.			
JY		5,453,384	09/26/95	Chatterjee			

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		5,225,702	07/06/1993	Chatterjee			
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		5,807,791	09/15/98	Bertin et al			
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JY		5,654,862	08/05/97	Worley et al.			

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